CLAIMS: We claim:

1. A method for implementing coprocessor architecture in control processors using synchronous logic design technique to achieve digital signal processing capability, said method comprising the steps of:

   implementing signed two's complement multiplication function; and

   implementing divide function; and

   implementing shift left and shift right function; and

   implementing normalization function.

2. A method of implementing coprocessor architecture using register file as the interface for selecting the desired math computation.

3. A method of implementing coprocessor architecture using source data dependency to compute the time duration required to perform the math computation.